ece340_lab5

Dan White

October 30, 2014

Part I

FET transistors

This lab investigates the triode mode characteristics of the MOSFET and an application as a logic inverter.

1 Introduction

The drain current in a MOSFET in *linear* or *triode* mode can be expressed as:

$$i_D(tri) = K_n \left[(v_{GS} - V_{TN}) v_{DS} - \frac{v_{DS}^2}{2} \right]$$

where $K_n = \mu_n C_{ox} \frac{W}{L}$ is in units of $\mathrm{A/V^2}$ and can be considered a constant. For small v_{DS} values, defined as $v_{DS} \ll v_{GS} - V_T$, the squared term is very small and the equation may be approximated as:

$$i_D(tri) \approx K_n (v_{GS} - V_{TN}) v_{DS}$$

This drain current has an approximately linear relationship on both v_{GS} and v_{DS}. Since the drain terminal is involved in both the current flow and its value, it is useful to view the gate-source voltage as the controlling voltage.

The derivative of this current with respect to changes in drain-source voltage gives:

$$\frac{d\, i_D}{d\, v_{DS}} \approx K_n (v_{GS} - V_{TN})$$

This has units of conductance ($\mathrm{A/V}$). With a 2-level waveform (square wave) for v_{GS}, this transistor works like a switch. Its inverse is called the transistor's *on* resistance:

$$R_{DS,on} = \frac{1}{K_n (V_{GS} - V_{th})}$$

2 Experiment

2.1 FET as a voltage-controlled resistor

Construct the circuit shown in **Figure 1**. Measure the resistance with a multimeter between the FET's drain and source terminals as a function of the applied v_{GS} voltage. Vary the gate-source voltage from zero to a maximum of $15\,\mathrm{V}$ (the FETs used here have a maximum v_{GS} of $20\,\mathrm{V}$ determine the step sizes to obtain a smooth plot around the threshold voltage. At low v_{GS} voltages, the D-S terminals will behave like an open-circuit, increase the gate voltage until the multimeter just begins to measure a high, but in-range, resistance. Be sure to use the appropriate resistance range on the multimeter for each measurement to obtain the most digits of precision. Do this for both the **BS170** and **IRFZ44N** n-channel FETs.

Use the circuit of **Figure 2** and do the same procedure for the **IRF9Z34N** p-channel FET.

2.2 NMOS inverter

Construct the circuit of **Figure 3**. Apply a $100\,\mathrm{kHz}$, 0 to $5\,\mathrm{V}$ square wave as v_{in}. Monitor both v_{in} and v_{out} on an oscilloscope. Measure the delay between the 50% points $(2.5\,\mathrm{V})$ of the waveforms, this is the inverter's delay. Also measure the 10-90% rise and fall times of the two waveforms.

2.3 Analysis

Voltage-controlled resistor:

- Plot the R_{DS} versus v_{GS} curves for the three transistors on the same plot.
- Estimate each device's threshold voltage V_{TN} or V_{TP} and compare to the datasheet values.
- Estimate the values of K_n for the **BS170** and **IRFZ44N** transistors.

Inverter:

- Can you estimate the output's rise and fall times from the circuit and the datasheet values? Notice that the waveforms have the shape of R-C exponentials.