ece340_lab7

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Part I

CMOS logic gates

This lab's purpose is to provide hands-on practice at implementing arbitrary logic functions in the CMOS circuit style. It exercises independent design and critical thinking skills in an open-ended lab procedure.

1 Introduction

CMOS logic gates can implement near-arbitrary logic functions in a single gate design. Functions directly implementable have non-complemented inputs and are inverting in nature. In their canonical from, these use a sum-of-products with an overall inversion. Logic functions which use inverted inputs or a non-inverted ouput are generated simply by placing additional inverters in the circuit. In this way, any logic function can be realized with a single core gate and inverters.

Because of this capability, libraries of "standard cells" are constructed and provided by companies for building-block digital logic design on CMOS integrated circuits. Besides the normal 2 or 3-input logic gates, other functions like AND-OR-INVERT (AOI) are provided to reduce the overall implementation area. AOI gates are 3 or more input functions represented as a sum-of-products, a simple version being `Y = (AB + C)'`.

2 Experiment

Obtain your specific logic function to implement from your instructor.

Design the schematic for a CMOS logic gate which implements this function. Since we are not implementing these gates on an integrated circuit, you do not have control over the transistor sizes.

Work out the truth table for this design, considering the MOSFETs as switches to verify your design.

Construct a CMOS inverter on a protoboard with a $10\,\mathrm{nF}$ capacitor as the load. Re-measure the rise, fall, and delay times for this inverter exactly like Lab 6.

Construct your logic gate on a protoboard. Use the `BS170` N-MOS and either `BS250P` or `VP2016` P-MOS transistors.Include a $10\,\mathrm{nF}$ capacitor connected to the output as a load. Use wires connected to either V_{DD} or GND to verify the truth table of the circuit.

Measure the rise, fall, and delay times for this gate under all logic combinations and single-input changing state transitions. Can you predict the best- and worst-case delay times combinations? Do this by replacing one of the inputs with the signal generator and measuring the input/output waveforms as done in Lab 6.

3 Report

The report sections shall be structured as follows:

- **Procedure** - Record your design procedure and resulting schematic of the logic gate. Record your strategy for finding the various measurements on the inverter and your gate.
- **Results** - Record your measurements here
- **Analysis** - Record any extracted measurements or calculations. It is possible to predict your gate's transient performance from your measurements of the "base inverter" and the schematic of your new gate.
- **Discussion** - Discuss the reasons you chose a particular measurement procedure. Include comparisons from your predicted times and measured times for your gate. What differences are there? Can you refine your estimates to better match measured results?